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(54) **Method of manufacturing an amorphous-silicon thin film transistor**

(57) A method of manufacturing an amorphous-silicon thin film transistor comprising forming a gate electrode (2) on an insulating substrate (1); forming a gate insulating layer (3) on the gate electrode (2); forming an amorphous-silicon layer (4) on the gate insulating layer (3); forming a protective insulating layer (5) on the amorphous-silicon layer (4); exposing the amorphous-silicon layer (4), while ensuring that it overlaps at least part of the gate electrode (2), by selectively removing the protective insulating layer (5); forming on the protective insulating layer (5) and on the so-exposed amorphous silicon layer (4) an impurities-containing silicon layer (6) which contains impurities serving as a donor or an acceptor; forming a metal mask, (7) having a configuration corresponding to a source electrode and a drain electrode of the transistor, on the impurities-containing silicon layer (6); and using said mask (7) in the course of effecting simultaneous formation both of the exterior periphery of the transistor and of the final shape of the impurities-containing silicon layer (6).

FIG. 1

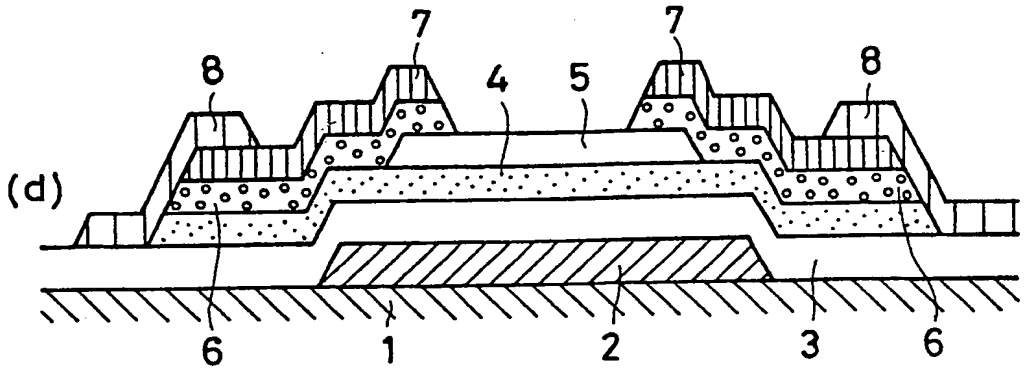

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FIG. 1

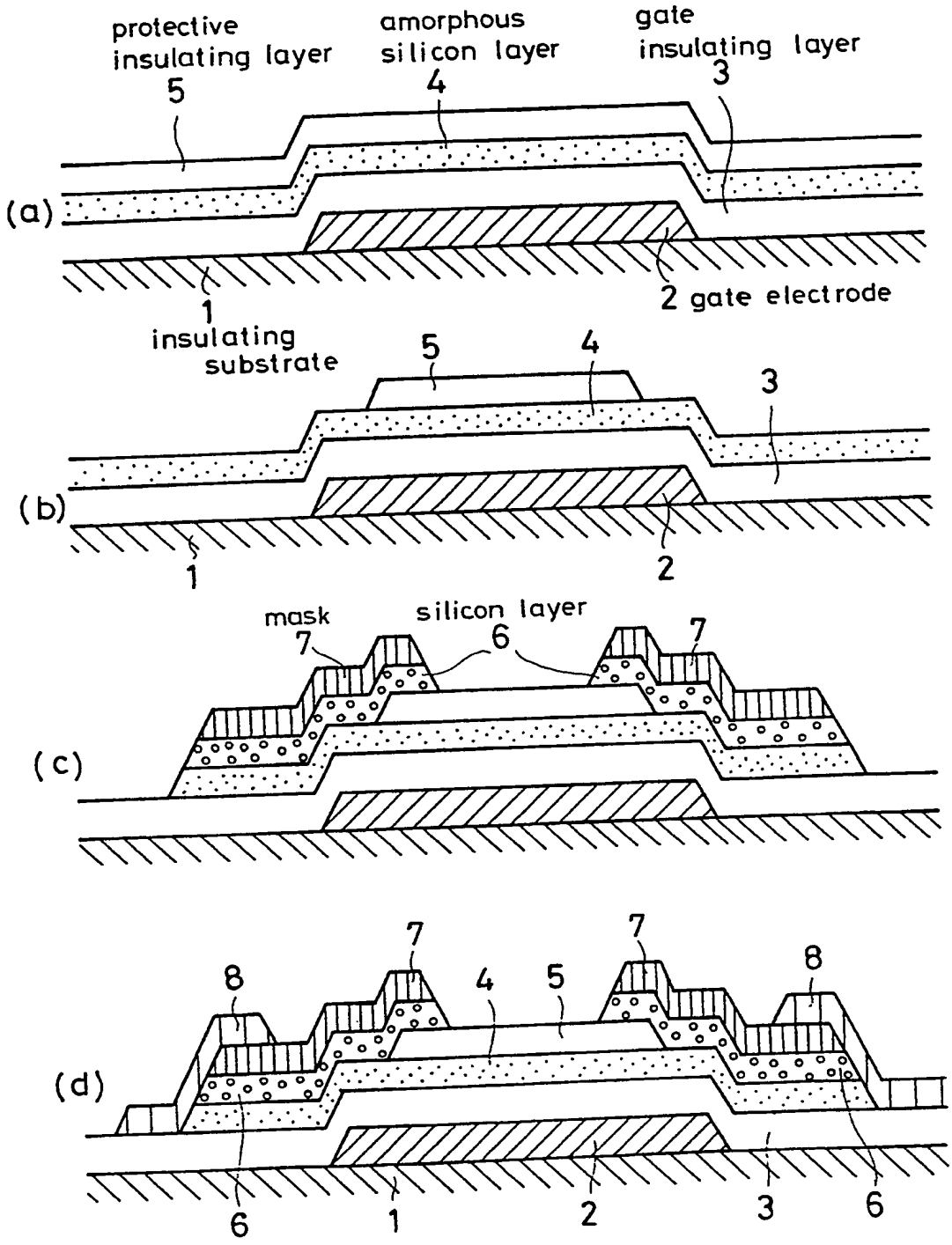

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FIG. 2

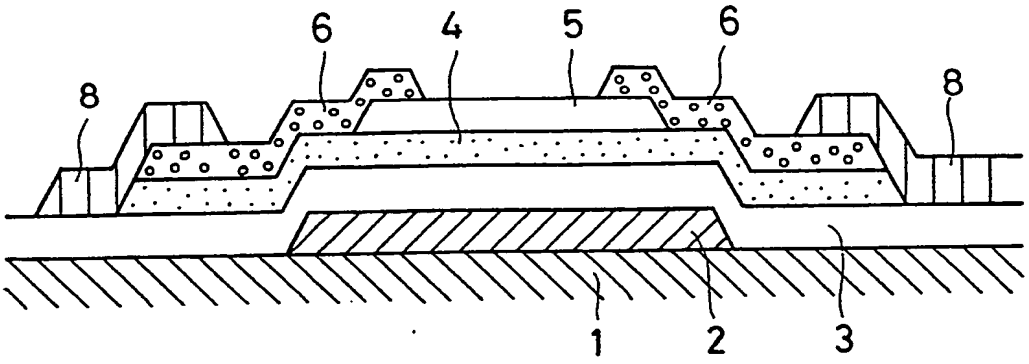

FIG. 4

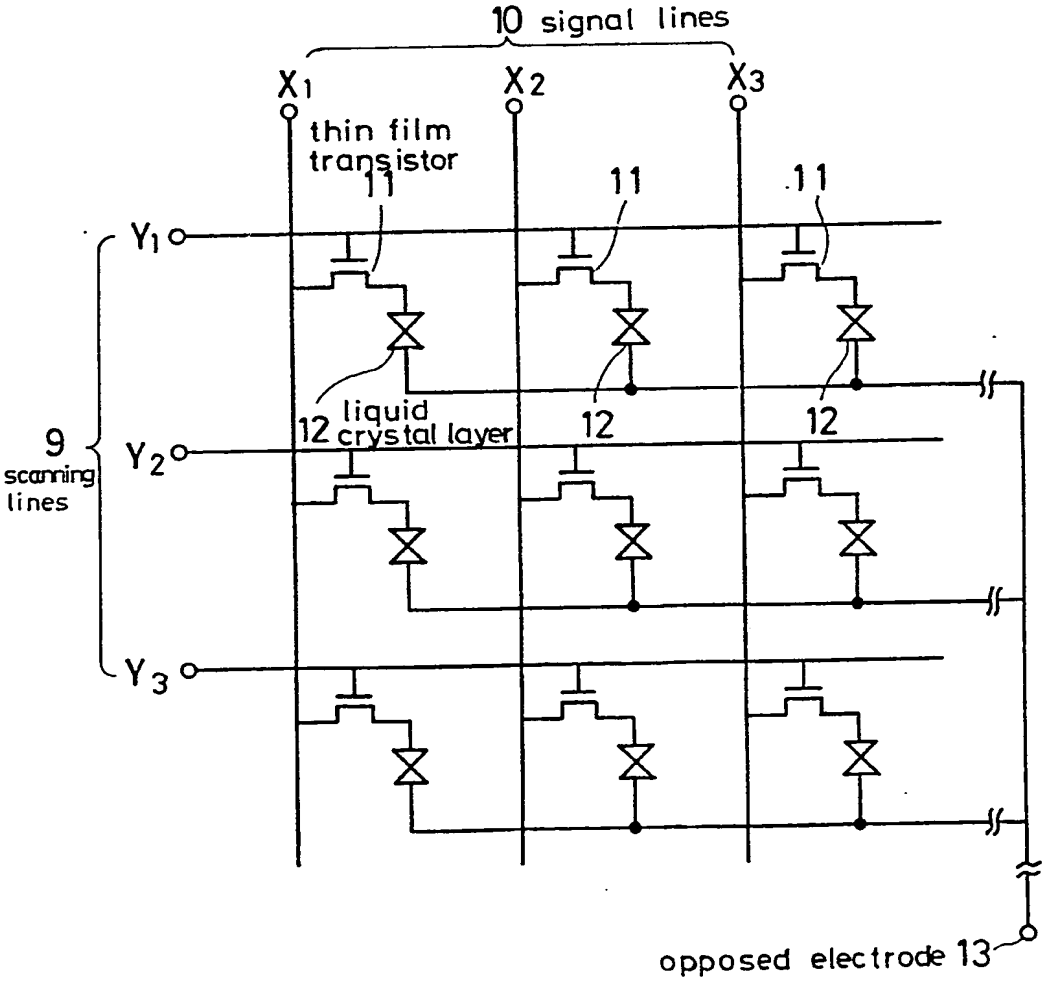

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FIG. 3

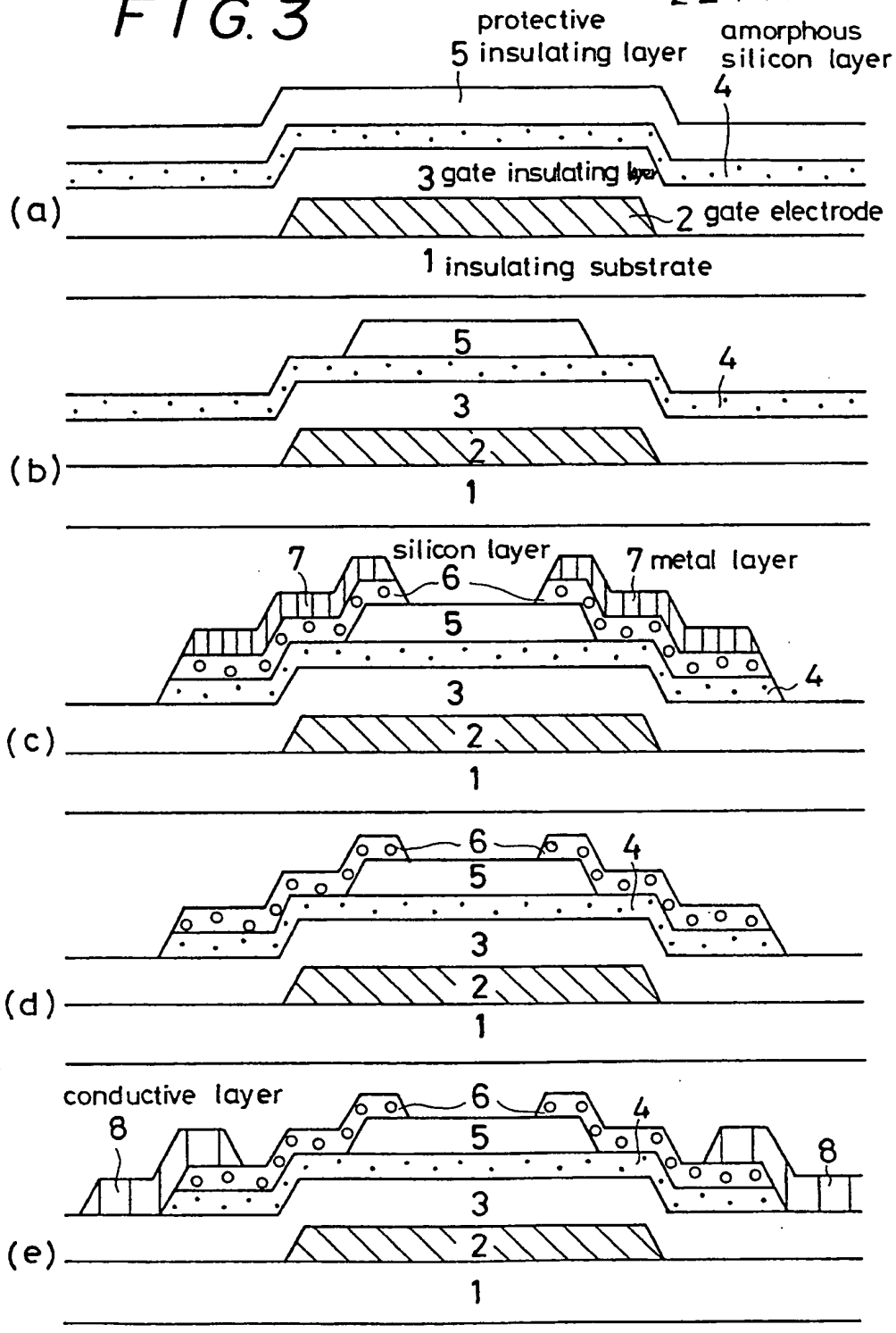

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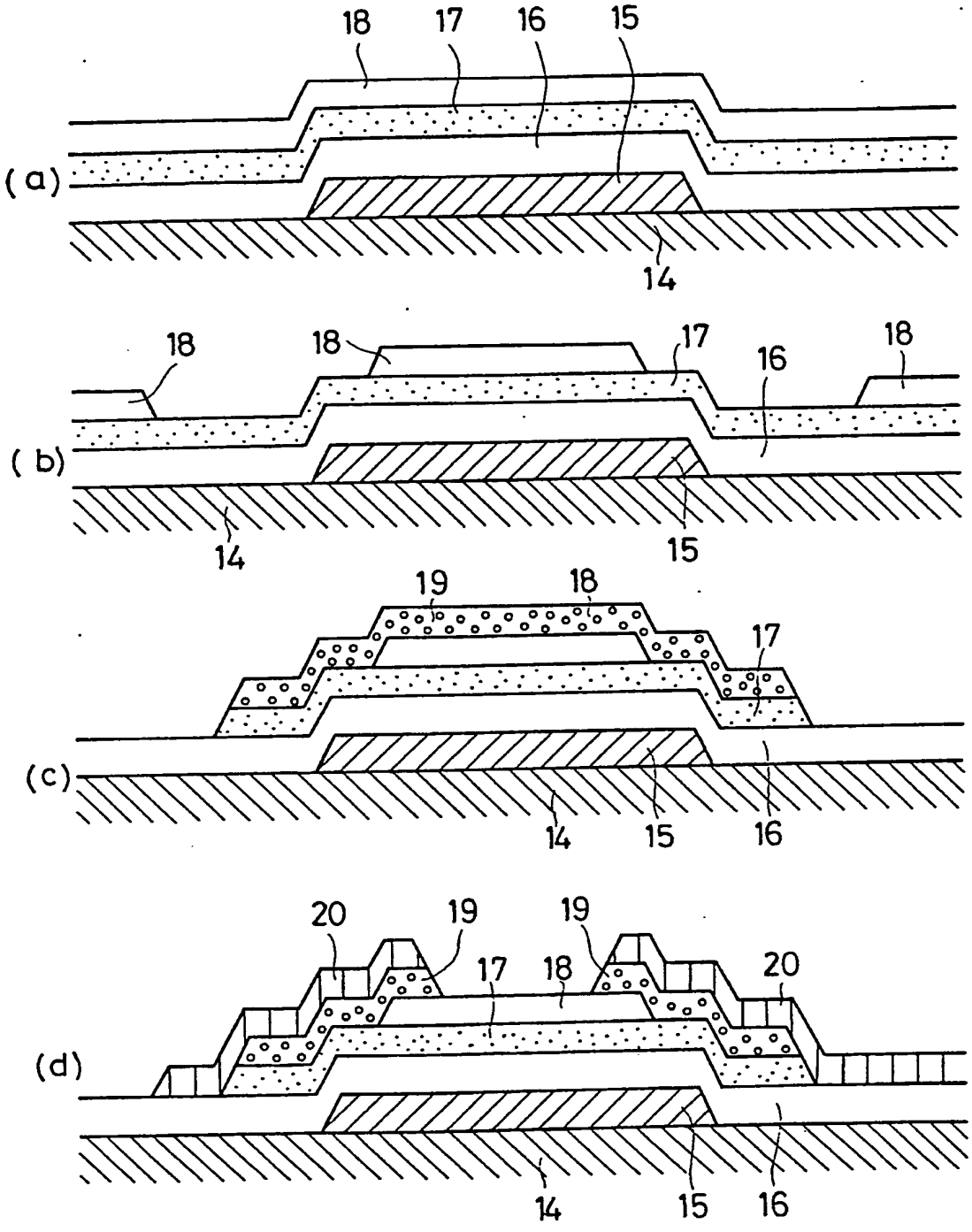
FIG. 5



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"METHOD OF MANUFACTURING AN AMORPHOUS-SILICON THIN FILM TRANSISTOR"

This invention concerns a method of manufacturing an amorphous-silicon thin film transistor and a transistor made by such a method.

According to the present invention, there is provided a method of manufacturing an amorphous-silicon thin film transistor comprising forming a gate electrode on an insulating substrate; forming a gate insulating layer on the gate electrode; forming an amorphous-silicon layer on the gate insulating layer; forming a protective insulating layer on the amorphous-silicon layer; exposing the amorphous-silicon layer, while ensuring that it overlaps at least part of the gate electrode, by selectively removing the protective insulating layer; forming on the protective insulating layer and on the so-exposed amorphous silicon layer an impurities containing silicon layer which contains impurities serving as a donor or an acceptor; forming a mask, having a configuration corresponding to a source electrode and a drain electrode of the transistor, on the impurities-containing silicon layer; and using said mask in the course of effecting simultaneous formation both of the exterior periphery of the transistor and of the final shape of the impurities-containing silicon layer.

Preferably the mask is constituted by a metal layer.

Preferably, after the said use of the mask, the mask is removed so as to expose the source electrode and the drain electrode.

A conductive layer may be formed so as to contact the impurities-containing silicon layer and the amorphous-silicon layer.

The conductive layer may be formed after removal of the mask.

The conductive layer may be formed of indium tin oxide.

The said simultaneous formation may be effected by employing an organic alkali type solution to effect partial removal of the amorphous-silicon layer and of the impurities-containing silicon layer.

The invention also comprises an amorphous-silicon thin film transistor which has been produced by the method set forth above.

The invention is illustrated merely by way of example, in the accompanying drawings, in which:-

Figures 1(a) to 1(d) constitute sectional views of a product at successive stages of a method according to the present invention of manufacturing an amorphous-silicon thin film transistor,

Figure 2 is a sectional view of another product which may be made by the method according to the present invention,

Figures 3(a) to 3(e) are views similar to those of Figures 1(a) to 1(d) but illustrating another embodiment of the present invention;

Figure 4 is an electrical circuit diagram showing the construction of an active matrix type liquid crystal display; and

Figures 5(a)-5(d) constitute sectional views of a product at successive stages of a known method of manufacturing an amorphous-silicon thin film transistor.

A liquid crystal matrix display is known in which an MIS-type thin-film transistor using amorphous-silicon is provided for each pixel as the switching element. Such a display is known as an active matrix type liquid crystal display and is used as a thin type image display.

Figure 4 shows an example of the construction of the above-described active matrix type liquid crystal display. When, for example, a scanning line Y_1 is selected from among a group of scanning lines 9, the gates of thin-film transistors 11 connected thereto are simultaneously turned on, and through the sources of the thin-film transistors 11 which have been thus turned on, a signal voltage corresponding to image information is transmitted

from each signal line of a group of signal lines 10 to the drain of each thin film transistor 11. Connected to each drain is a pixel electrode (not shown), images being displayed by varying the light transmittance of a liquid crystal layer 12 through the voltage difference between the pixel electrode and an opposed electrode 13 formed on a substrate on the opposite side with respect to the liquid crystal layer 12. After the above-mentioned gate is turned off, the voltage difference between the above-mentioned pixel electrode and the opposed electrode 13 is retained until the scanning line Y_1 is selected for the next time, so that the liquid crystal corresponding to each pixel is static-driven, thus achieving a high-contrast image display.

Japanese Laid-Open Patent Specification No. 58-212177 discloses a method of manufacturing thin-film transistors 11 in which a gate insulating layer, an amorphous-silicon layer, and a protective insulating layer are successively formed in such a way as to ensure the reliability and reproducibility of the manufacturing process.

Figure 5 illustrates the above-mentioned known manufacturing process.

First a gate electrode 15 is formed on an insulating substrate 14 of glass or the like. Then,a gate insulating layer 16, an amorphous-silicon layer 17, and a protective

insulating layer 18 are successively formed one on top of the other as shown at (a).

Subsequently, openings are made in the protective insulating layer 18 so that the latter only partly overlaps the gate electrode 15, thus exposing the amorphous-silicon layer 17, as shown at (b).

Then, a silicon layer 19 which contains impurities serving as a donor or an acceptor is formed. The silicon layer 19, the protective insulating layer 18, and the amorphous-silicon layer 17 are selectively removed, thereby forming an island structure defined in part by said openings, as shown at (c).

Subsequently, a transparent conductive layer 20 is formed over the said island structure, and is selectively removed in such a way as to form a source, a drain electrode pattern, a source wiring pattern, and a pixel electrode pattern. The silicon layer 19 is then removed using the pattern of the transparent conductive layer 20 as a mask, as shown at (d).

In the method illustrated in Figure 5, the silicon layer 19 undergoes etching twice, i.e. in the process steps (c) and (d), which is not desirable in terms of production time and cost.

Further, when forming an island structure in the above process as shown at (c), photo-resist is used as an

etching mask, which involves the following problems:-

First, since a wet etching method cannot be adopted, it is difficult to increase production throughput.

Second, since the photo-resist is directly applied to the silicon layer 19, the surface of the silicon layer 19 after the photo-resist has been peeled off is not sufficiently clean, so that it is difficult to form a satisfactory contact between this layer and a metal layer which is to be formed in the subsequent process.

The present invention therefore aims to provide a method of manufacturing amorphous-silicon thin-film transistors in which the number of process steps is reduced, the production throughput is increased, and a stabilization of the properties of the products is achieved.

A first embodiment of this invention will now be described with reference to Figure 1.

First, a gate electrode 2, made of a metal such as Cr, is formed on an insulating substrate 1 of glass or the like. Then, a gate insulating layer 3 of silicon nitride or silicon oxide, an amorphous-silicon layer 4, and a protective insulating layer 5 of silicon nitride or silicon oxide are successively formed by, for example, the plasma CVD (chemical vapour deposition) method, as shown at (a).

Next, selective etching of the protective insulating

layer 5 is conducted using a buffering hydrofluoric acid solution, thus exposing the amorphous-silicon layer 4 in such a manner that it overlaps the gate electrode 2 at least partly, as shown at (b).

Then, an impurities-containing silicon layer 6 containing an appropriate amount of phosphoros as impurities and a metal layer or mask 7 made of Ti or the like are successively formed on top of one another, the impurities-containing silicon layer 6 containing impurities which serve as a donor or an acceptor and being disposed on the protective insulating layer 5. When Ti is used for the metal layer or mask 7, selective etching of the metal layer or mask 7 is conducted using an aqueous solution of hydrofluoric nitric acid. A pattern corresponding to a source electrode and a drain electrode is then imparted to the metal layer or mask 7. Then by using the mask 7,etching of the impurities-containing silicon layer 6 to its final shape and etching of the amorphous-silicon layer 4 is performed using an organic alkali solution such as PAW (pyrocatechol diamine water), thereby simultaneously forming an island structure on which the source electrode and the drain electrode are formed, as shown at (c), and thus forming the exterior periphery of the transistor.

Subsequently, a transparent conductive layer 8 of ITO (indium tin oxide) or the like is formed. When ITO is used

for the transparent conductive layer 8, selective etching of the transparent conductive layer 8 is conducted using a ferric chloride type solution, thereby forming a source wiring connected to the source electrode and a pixel electrode connected to the drain electrode,this step being shown at (d).

In the manufacturing method illustrated in Figure 1, the etching of the impurities-containing silicon layer 6 is effected in the course of a single process step (c) which leads to a reduction in the number of process steps, an increase in the production throughput, and a stabilization of the properties of the product.

When forming the island structure on which the source electrode and the drain electrode are formed, photo-resist may be adopted instead of the metal layer 7. A pattern corresponding to the source and the drain will then be imparted to the photo-resist etching of the impurities-containing silicon layer 6 and the amorphous-silicon layer 4 being conducted using the pattern as the mask. In that case, however, a dry etching method using a CF_4 type gas must be adopted, since an organic alkali type solution would attack the photo-resist when used for etching of the impurities-containing silicon layer 6 and the amorphous-silicon layer 4.

Figure 2 shows the section of a different amorphous-silicon thin-film transistor which can be manufactured by the method

of the present invention.

A further embodiment of this invention will now be described with reference to Figure 3.

This embodiment is characterized in the latter part of the production processes. The processes illustrated in Figures 3(a) through 3(c) being the same as those shown in Figures 1(a) through 1(c), an explanation will only be given of the processes illustrated in Figures 3(d) through 3(e), parts shown in Figure 3 which correspond to like parts in Figure 1 being given the same reference numerals.

The impurities-containing silicon layer 6 is exposed by removing the metal layer 7 using an aqueous solution of weak fluoric nitric acid, as shown at (d).

The conductive layer 8 is formed using ITO, which conductive layer 8 is selectively removed using a ferric chloride type solution as indicated at (e), thereby forming a source wiring connected to the source electrode and a pixel electrode connected to the drain electrode.

As described above, the conductive layer 8 has only the step section between the two layers of the amorphous-silicon layer 4 and the impurities-containing silicon layer 6 to cover. In the first embodiment shown in Figure 1, the conductive layer 8 covers the step sections connecting the three layers of the amorphous-silicon layer 4, the impurities-containing silicon layer 6 and the metal

layer 7, with each other. Consequently, the conductive layer 8 in the Figure 3 embodiment can cover the step section more effectively than that in the first embodiment shown in Figure 1, resulting in a reduced possibility of disconnection occurring.

A similar process to that described above can also be adopted when connecting other conductive layers than the conductive layer 8 of ITO to the impurities-containing silicon layer 6 serving as the source electrode and the drain electrode.

In the embodiments described above, the impurities-containing silicon layer 6 and the amorphous silicon layer 4 can simultaneously undergo etching. As a result, the production processes can be shortened and an improvement in the manufacturing yield is to be expected.

Further, by employing a metal layer 7 as the mask for forming an island structure on which the source electrode and the drain electrode are formed, a wet etching method using an organic alkali type solution can be adopted for the etching of the impurities-containing silicon layer 6 and the amorphous-silicon layer 4. Consequently, the production processes can achieve a higher throughput. Moreover, since the surface of the impurities-containing silicon layer 6 is not directly exposed to the photo-resist, a satisfactory contact can be achieved between the said surface and the metal of the source electrode and the drain electrode, so that

stabilization of the properties of the product is to be expected.

Furthermore, in the case of a product whose conductive layer 8 covers a step section between the two layers 4, 6 only, the step section can be covered more effectively, which leads to a reduced possibility of disconnection occurring as well as to an improvement in manufacturing yield.

CLAIMS

1. A method of manufacturing an amorphous-silicon thin film transistor comprising forming a gate electrode on an insulating substrate; forming a gate insulating layer on the gate electrode; forming an amorphous-silicon layer on the gate insulating layer; forming a protective insulating layer on the amorphous-silicon layer; exposing the amorphous-silicon layer, while ensuring that it overlaps at least part of the gate electrode, by selectively removing the protective insulating layer; forming on the protective insulating layer and on the so-exposed amorphous silicon layer an impurities-containing silicon layer which contains impurities serving as a donor or an acceptor; forming a mask, having a configuration corresponding to a source electrode and a drain electrode of the transistor, on the impurties-containing silicon layer; and using said mask in the course of effecting simultaneous formation both of the exterior periphery of the transistor and of the final shape of the impurities-containing silicon layer.

2. A method as claimed in claim 1 in which the mask is constituted by a metal layer.

3. A method as claimed in claim 1 or 2 in which, after the said use of the mask, the mask is removed so as to expose the source electrode and the drain electrode.

4. A method as claimed in any preceding claim in which a conductive layer is formed so as to contact the impurities-containing silicon layer and the amorphous-silicon layer.

5. A method as claimed in claim 4 in which the conductive layer is formed after removal of the mask.

6. A method as claimed in claim 4 or 5 in which the conductive layer is formed of indium tin oxide.

7. A method as claimed in any preceding claim in which the said simultaneous formation is effected by employing an organic alkali type solution to effect partial removal of the amorphous-silicon layer and of the impurities-containing silicon layer.

8. A method of manufacturing an amorphous-silicon thin film transistor substantially as hereinbefore described with reference to any of Figures 1-3.

9. An amorphous-silicon thin film transistor which has been produced by the method claimed in any preceding claim.

10. Any novel integer or step, or combination of integers or steps, hereinbefore described and/or as shown in the accompanying drawings, irrespective of whether the present claim is within the scope of, or relates to the same or a different invention from that of, the preceding claims.

11. A method of manufacturing amorphous-silicon thin-film transistors, comprising the steps of:

forming a gate insulating layer on an insulating substrate on which a gate electrode is formed;

forming an amorphous-silicon layer on this gate insulating layer;

forming a protective insulating layer on this amorphous-silicon layer;

exposing said amorphous-silicon layer by selectively removing this protective insulating layer in such a manner that said amorphous-silicon layer overlaps at least part of the pattern of said gate electrode;

coating said protective insulating layer and said amorphous-silicon layer with a silicon layer containing impurities serving as the donor or the acceptor;

forming a mask having a configuration corresponding to the source electrode and the drain electrode on said silicon layer containing impurities and removing said silicon layer containing said impurities and said amorphous-silicon layer by means of said mask.

12. A method of manufacturing amorphous-silicon thin-film transistors, comprising the steps of:

forming a gate insulating layer on an insulating substrate on which a gate electrode is formed;

forming an amorphous-silicon layer on this gate insulating layer;

forming a protective insulating layer on this amorphous-silicon layer;

exposing said amorphous-silicon layer by selectively removing this protective insulating layer in such a manner that said amorphous-silicon layer overlaps at least part of the pattern of said gate electrode,

successively forming a silicon layer containing impurities serving as the donor or the acceptor and a metal layer;

imparting a pattern corresponding to the source electrode and the drain electrode to said metal layer;

removing said silicon layer and said amorphous-silicon layer, using said metal layer thus equipped with said pattern at the mask;

removing said metal layer so as to expose the source electrode and the drain electrode formed with said silicon layer; and connecting a conductive layer to the source electrode and the drain electrode thus exposed.

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